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BLAKELY SOKOLOFF TAYLOR & ZAFMAN
12400 WILSHIRE BOULEVARD
SEVENTH FLOOR
LOS ANGELES, CA 90025-1030

EXAMINER	
SIDDIQUI, SAQIB JAVAID	
ART UNIT	**PAPER NUMBER**
2138	

DATE MAILED: 04/03/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/815,217	ZIMMERMAN ET AL.	
	Examiner	Art Unit	
	Saqib J. Siddiqui	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 August 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-29* is/are rejected.

7)☒ Claim(s) *10 and 11* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Oath/Declaration

The Oath filed April 06, 2004 complies with all the requirements set fort in MPEP 602 and therefore is accepted.

Drawings

The filed drawings are accepted.

Specification

The disclosure is objected to because of the following informalities:

The following guidelines illustrate the preferred layout for the specification of a utility application. These guidelines are suggested for the applicant's use.

Arrangement of the Specification

As provided in 37 CFR 1.77(b), the specification of a utility application should include the following sections in order. Each of the lettered items should appear in upper case, without underlining or bold type, as a section heading. If no text follows the section heading, the phrase "Not Applicable" should follow the section heading:

(a) TITLE OF THE INVENTION.
(b) CROSS-REFERENCE TO RELATED APPLICATIONS.
(c) STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT.
(d) THE NAMES OF THE PARTIES TO A JOINT RESEARCH AGREEMENT
(e) INCORPORATION-BY-REFERENCE OF MATERIAL SUBMITTED ON A COMPACT DISC (See 37 CFR 1.52(e)(5) and MPEP 608.05. Computer program listings (37 CFR 1.96(c)), "Sequence Listings" (37 CFR 1.821(c)), and tables having more than 50 pages of text are permitted to be submitted on compact discs.) or
REFERENCE TO A "MICROFICHE APPENDIX" (See MPEP § 608.05(a). "Microfiche Appendices" were accepted by the Office until March 1, 2001.)
(f) BACKGROUND OF THE INVENTION.
(1) Field of the Invention.
(2) Description of Related Art including information disclosed under 37 CFR 1.97 and 1.98.

(g) **BRIEF SUMMARY OF THE INVENTION.**
(h) **BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING(S).**
(i) DETAILED DESCRIPTION OF THE INVENTION.
(j) CLAIM OR CLAIMS (commencing on a separate sheet).
(k) ABSTRACT OF THE DISCLOSURE (commencing on a separate sheet).
(l) SEQUENCE LISTING (See MPEP § 2424 and 37 CFR 1.821-1.825. A "Sequence Listing" is required on paper if the application discloses a nucleotide or amino acid sequence as defined in 37 CFR 1.821(a) and if the required "Sequence Listing" is not submitted as an electronic document on compact disc).

Appropriate correction is required.

Claim Objections

Claims 10-11 are objected to because of the following informalities:

As per claim 10:

This claims refers to "clam" (lines 1), whereas it should read claim. Applicant should insert an "i".

As per claims 11:

This claim is objected to by virtue of their dependency.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al. US PG-Pub no. 2002/0125879 A1.

As per claim 1:

Lee et al. substantially teaches an electronic system (Figure 4) comprising: a first memory module having a first memory array (Figure 3 # 34, paragraph [0035]) and a first buffer logic coupled to the first memory array (Figure 4 # 42); and a second memory module having a second memory array (Figure 3 # 35, paragraph [0035]) and a second buffer logic coupled to the second memory array (figure 4 # 43), and transmits a test pattern to the first memory module to carry out a test of the first memory module independently of the memory controller (paragraph [0038]).

Lee et al. does not explicitly teach the first buffer logic to be "directly" coupled to the second buffer logic.

However, it would be obvious to one with ordinary skill in the art to recognize that second buffer logic is further coupled the first buffer logic of the first memory module, via the parallel test slots (Figure 4 # 36 & 38), and via the reference slot (Figure 4 # 34).

Hence, the second buffer is indirectly coupled to the first buffer. In addition, it is merely within the workable range.

As per claim 2:

Lee et al. teaches an electronic system as rejected in claim 1 above further comprising: a memory controller coupled to the second buffer logic (Figure 4 # 10); and a processor (Figure 4 # 40) coupled to the memory controller to execute instructions stored in the second memory array of the second memory module under the control of the memory controller (paragraph [0037-0038]).

As per claim 3:

Lee et al. teaches an electronic system as rejected in claim 2 above, wherein the memory controller transmits a command to the second buffer logic (paragraph [0038]) under the control of the processor to cause the second buffer logic to carry out a test of the first memory module (paragraph [0037]).

As per claim 4:

Lee et al. teaches an electronic system as rejected in claim 3 above, further comprising a memory bus coupling together the memory controller, the first memory module and the second memory module (Figure 4, "data (I/O)"), and wherein the test pattern is transmitted across the memory bus (paragraph [0038]).

As per claim 5:

Lee et al. teaches an electronic system as rejected in claim 1 above, further comprising a point-to-point bus coupling the second buffer logic of the second memory module to the first buffer logic of the first memory module (Figure 4 # 34), wherein the

test pattern is transmitted by the second buffer logic across the point-to-point bus to the first buffer logic (paragraph [0035-0036]).

Lee et al. does not explicitly teach the first buffer logic to be "directly" coupled to the second buffer logic.

However, it would be obvious to one with ordinary skill in the art to recognize that second buffer logic is further coupled the first buffer logic of the first memory module, via the parallel test slots (Figure 4 # 36 & 38), and via the reference slot (Figure 4 # 34). Hence, the second buffer is indirectly coupled to the first buffer. In addition, it is a mere rearranging of parts.

As per claim 6:

Lee et al. teaches the electronic system as rejected in claim 1 above, further comprising a test source coupled to the second buffer logic (Figure 4 # 10), wherein the test source transmits a command to the second buffer logic to cause the second buffer logic to carry out a test of the first memory module (paragraph [0038]).

As per claim 7:

Lee et al. teaches the electronic system as rejected in claim 6 above, further comprising a serial bus coupling the second buffer logic to the test source (Figure 4 "data (I/O)"), wherein the command is transmitted by the test source across the serial bus to the second buffer logic (paragraph [0038]).

As per claim 8:

Lee et al. teaches the electronic system as rejected in claim 6 above, wherein the test pattern is received by the second buffer logic from the test source (claim 7).

Lee et al. discloses the claimed invention except for the test patterns are stored in the buffer and transmitted from the buffer as opposed to the memory. It would have been obvious to one having ordinary skill in the art at the time the invention was made to store the test patterns in the memory and transmit them to the other memory from the first memory, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller,* 105 USPQ 233.

As per claim 9:

Lee et al. teaches the electronic system as rejected in claim 1 above, wherein the test pattern is generated by the second buffer logic in response to commands received by the second buffer logic (paragraph [0038]).

Lee et al. discloses the claimed invention except for the test patterns are stored in the buffer and transmitted from the buffer as opposed to the memory. It would have been obvious to one having ordinary skill in the art at the time the invention was made to store the test patterns in the memory and transmit them to the other memory from the first memory, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller,* 105 USPQ 233.

As per claim 10:

Lee et al. teaches the electronic system as rejected in claim 1 above, wherein the test pattern incorporates commands for the first buffer logic to carry out (paragraph [00338]).

As per claim 11:

Lee et al. teaches the electronic system as rejected in claim 10 above.

Lee et al. discloses the claimed invention except for the test patterns incorporating a deliberately created error. It would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate a deliberately created error to elicit an expected action, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller,* 105 USPQ 233.

As per claim 12:

Lee et al. teaches the electronic system as rejected in claim 1 above, further comprising an analysis module having a third buffer logic (Figure 4 # 45) having an interface to couple the third buffer logic to an analysis device (figure 4 # 45), the second buffer logic is coupled to the third buffer logic (Figure 4) and the third buffer logic is coupled to the first buffer logic (Figure 4 "data (I/O)").

Lee et al. discloses the claimed invention except for the third buffer is not interposed between the first buffer and the second buffer, and also the test patterns are not passed through the third buffer. It would have been obvious to one having ordinary skill in the art at the time the invention was made to interpose the third buffer between the first and the second buffer, and to pass the test pattern through the third buffer, since it has been held that rearranging parts of an invention involves only routine skill in the art. *In re Japikse,* 86 USPQ 70. It would have also been obvious to one having ordinary skill in the art at the time the invention was made, since it has been held that

where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller,* 105 USPQ 233.

As per claim 13:

Lee et al. teaches the electronic system as rejected in claim 12 above, further comprising: a first point-to-point bus coupling the first buffer logic of the first memory module to the third buffer logic (Figure 4, "data (I/O)"); and a second point-to-point bus coupling the second buffer logic of the second memory module to the third buffer logic (Figure 4).

As per claim 14:

Lee et al. teaches the electronic system as rejected in claim 12 above, wherein the third buffer logic provides an indication to an analysis device of the transmission of the test pattern by the second buffer logic to the first buffer logic (paragraph [0037-0038]), and wherein the third buffer logic provides an indication to an analysis device of a signal transmitted by the first buffer logic in response to the carrying out of a test by the second buffer logic and indicating a status of the test (paragraph [0039-0040]).

As per claim 15:

Lee et al. teaches the electronic system as rejected in claim 12 above, wherein all three of the first buffer logic, the second buffer logic and the third buffer logic are integrated circuits of substantially similar design (Figure 4, page 3), and wherein the interface of the third buffer logic to couple the third buffer logic to an analysis device is of substantially the same design as both a corresponding interface of the first buffer

logic to couple the first buffer logic to the first memory array, and a corresponding interface of the second buffer logic to couple the second buffer logic the second memory array (Figure 4).

As per claim 16:

Lee et al. teaches a buffer logic comprising: a first point-to-point bus interface (Figure 4, "data (I/O)"); a second point-to-point bus interface (Figure 4, bus between DUT and buffer 45); an interface to a memory array (Figure 4 # 36 & 38); and test logic to transmit a test pattern through the first point-to-point interface to carry out a test of a memory module in response to the buffer logic receiving a command (paragraph [0038]).

Lee et al. does not explicitly teach the second point-to-point to be connected to the elements in the same way as the invention.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to change the location of the second point-to-point, since it has been held that rearranging parts of an invention involves only routine skill in the art. *In re Japikse,* 86 USPQ 70. It would have also been obvious to one having ordinary skill in the art at the time the invention was made, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller,* 105 USPQ 233.

As per claim 17:

Lee et al teaches the buffer logic as rejected in claim 16, except for the test patterns are stored in the buffer and transmitted from the buffer as opposed to the

memory. It would have been obvious to one having ordinary skill in the art at the time the invention was made to store the test patterns in the memory and transmit them to the other memory from the first memory, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller,* 105 USPQ 233.

As per claim 18:

Lee et al. teaches the buffer logic as rejected in claim 16, further comprising an interface to a configuration bus to which a test source may be attached (Figure 4 # 10), and from which the command may be received by the buffer logic from the test source (Figure 4 # 43).

As per claim 19:

Lee et al. teaches the buffer logic as rejected in claim 18, in which the buffer logic receives the test pattern from the test source (paragraph [0038]).

As per claim 20:

Lee et al. teaches the buffer logic as rejected in claim 18 in which the buffer logic generates the test pattern in response to at least one test command from the test source (paragraph [0038]).

As per claim 21:

Lee et al. teaches the buffer logic as rejected in claim 16, wherein the buffer logic is an integrated circuit attached to a circuitboard (Figure 3 # 30) of a first memory module to which memory ICs are also attached that form a first memory array to which the buffer logic is coupled (paragraph [0035]).

As per claim 22:

Lee et al. teaches the buffer logic as rejected in claim 21, wherein the first memory module is releasably connected to a circuitboard to which a second memory module is electrically coupled (paragraph [0042]), thereby electrically coupling the first and second memory modules (Figure 5), and wherein the buffer logic transmits the test pattern to the other memory module (Figure 4).

As per claim 23:

Lee et al. teaches the buffer logic as rejected in claim 22, wherein the buffer logic transmits the test pattern to test another buffer logic within the second memory module (Figure 4 # 38).

As per claim 24:

Lee et al. teaches the buffer logic as rejected in claim 22, wherein the buffer logic transmits the test pattern to test the second memory array (Figure 4 # 38).

As per claims 25-29:

Claims 25-29 are directed to a method of the system of and buffer logic of Claims 1-24. Lee et al. as stated above, teaches the system as set forth in Claims 1-24. Therefore, Lee et al. also teaches, the method as set forth in Claims 25-29.

Claims 1, 16 & 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Perego et al. US Patent no. 6,502,161 B1.

As per claim 1:

Perego et al. teaches the test system of the claimed invention (Figure 2B and 3B) except for it teaches only one buffer device. It would have been obvious to one having

ordinary skill in the art at the time the invention was made to use multiple buffer devices, since it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art. Further it should be noted, that Perego et al.'s invention performs the same function and it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller,* 105 USPQ 233.

As per claim 16:

Perego et al. teaches the buffer logic of the claimed invention (Figure 2B and 3B) except for it teaches only one buffer device. It would have been obvious to one having ordinary skill in the art at the time the invention was made to use multiple buffer devices, since it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art. Further it should be noted, that Perego et al.'s invention performs the same function and it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller,* 105 USPQ 233.

As per claim 25:

Perego et al. teaches the method of the claimed invention (Figure 2B and 3B) except for it teaches only one buffer device. It would have been obvious to one having ordinary skill in the art at the time the invention was made to use multiple buffer devices, since it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art. Further it should be noted, that Perego et al.'s invention performs the same function and it has been held that where the general

conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller,* 105 USPQ 233.

Examiner's Note: Examiner has cited particular columns and line numbers in the references as applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings in the art and are applied to the specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant, in preparing the responses, to fully consider the references in entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the examiner.

Related Art

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Additional pertinent prior arts, US PG Pub no. (20020056062 A1, 20030041086 A1) and US Pat no. (5852617 A) mention the same testing system wherein a buffer is employed to test memory modules.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Saqib J. Siddiqui whose telephone number is (571) 272-6553. The examiner can normally be reached on 8:00 to 4:30. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can

be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SS

Saqib Siddiqui

Art Unit 2138
03/17/2006

ALBERT DECADY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100